SPECIFICATIONS FOR LCD MODULE

MODEL NO.
BO2002A series
VER.01

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

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History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/05/12	SPEC.

CONTENTS

1. Numbering System

	B	O	2002	A	-	-	-	-	-	xxx
	0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	G=STN/gray Y=STN/yellow-green PLED/yellow-green C=color STN,OLED/RGB	B=STN/blue,OLED/blue F=FSTN T=TN D=OLED/blue+yellow A=OLED/blue+yellow+green
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB array I=RGB edge Q=LED edge/red N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on datasheet	t=temperature compensation for LCD p=touch panel $=RoHS

2. General Specification

(1) Mechanical Dimension

Item	Dimension	Unit
Number of Characters	20characters x 2 Lines	dots
Module dimension (L x W x H)	89.0 x 50.6 x 1.9 - no b/l	mm
View area	85.0 x 18.6	mm
Active area	73.5 x 11.5	mm
Character size	3.2x5.55	mm
Dot size	0.6x 0.65	mm
Dot pitch	0.67 x 0.7	mm

(2) Controller IC: ST7036i controller

(3) Temperature Range

	Normal	Wide
Operating	0 ~+50℃	-20 ~+70℃
Storage	-10 ~+60℃	-30 ~+80℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	0	-	+70	℃
Storage Temperature	T_{ST}	-30	-	+80	℃
Input Voltage	V_I	-0.3	-	Vdd+0.3	V
Supply Voltage For Logic	Vdd-Vss	-0.3	-	+7	V
Supply Voltage For LCD	Vo-Vss	-0.3+Vss	-	7-Vss	V

4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	—	2.7	3.0	4.5	V
Supply Voltage For LCD	Vo-Vss	＊Ta=-20℃ Ta=25℃ ＊Ta=+70℃	— — —	— 4.5 —	— — —	V
Input High Volt.	V_{IH}	—	1.9	—	Vdd	V
Input Low Volt.	V_{IL}	—	-0.3	—	0.2Vdd	V
Output High Volt.	V_{OH}	—	0.7*Vdd	—	—	V
Output Low Volt.	V_{OL}	—	—	—	0.8	V
Supply Current	Idd	Vdd=3.0V	160	—	230	uA

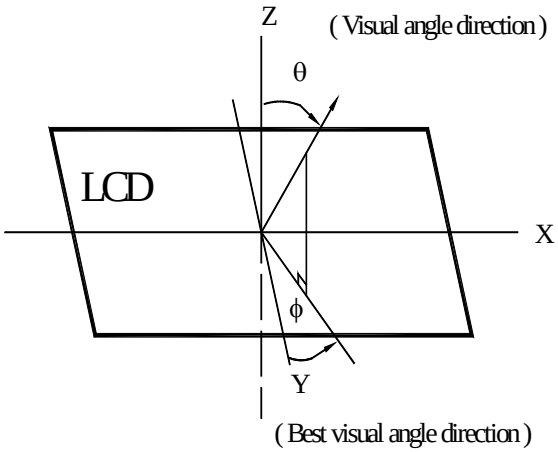
5. Optical Characteristics

a. STN

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧2	45	-	-	deg
	(H) ϕ	CR≧2	-	50	-	deg
Contrast Ratio	CR	-	2.0	6.0	-	-
Response Time 25℃	T rise	-	-	254	-	ms
	T fall	-	-	219	-	ms

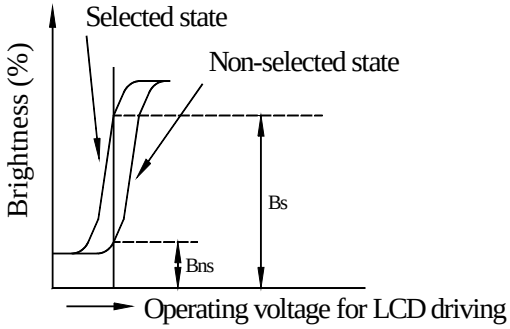
5.1 Definitions

■View Angles

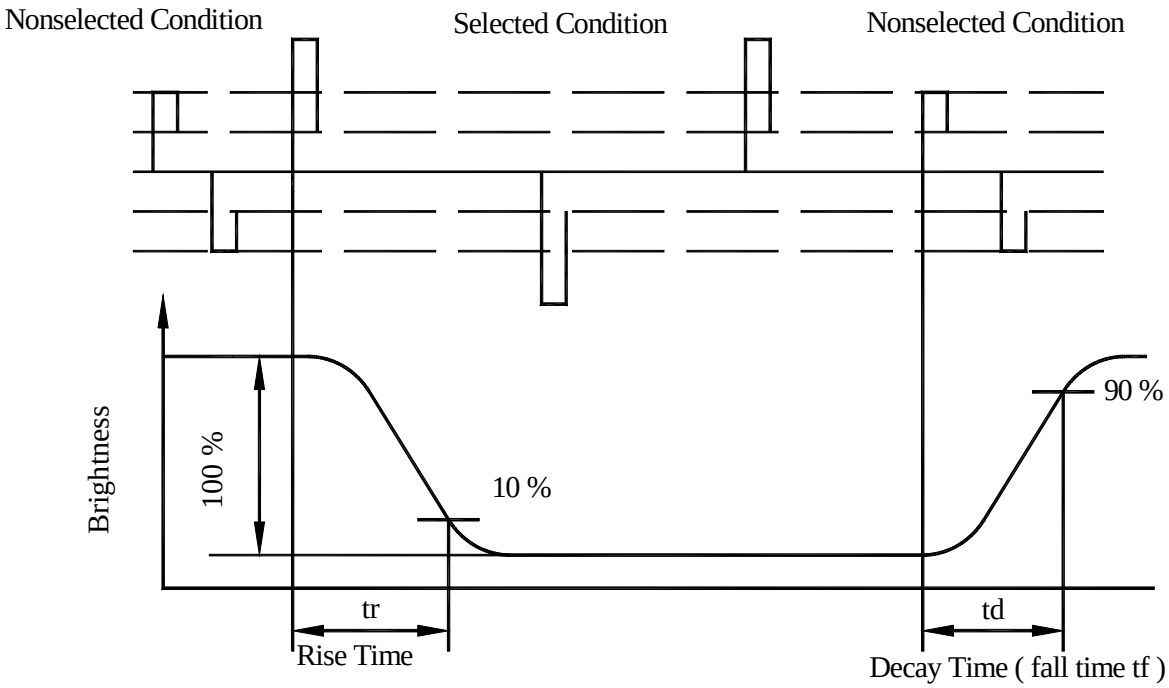


■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



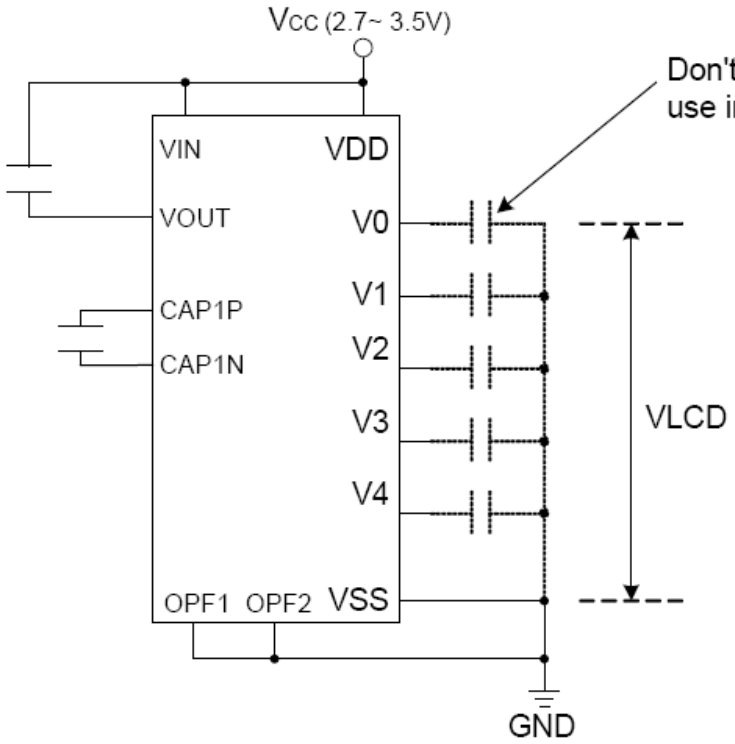
■Response Time

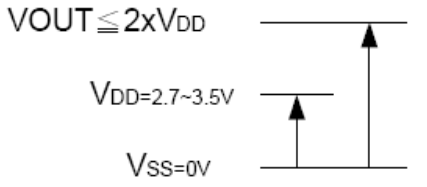


6. Interface Description

Pin No.	Symbol	Level	Description
1	VOUT	-	DC-DC voltage converter ,Connect a capacitor between this terminal And VIN when the built-in booster is used.
2	CAP-	-	For voltage booster circuit(VDD-VSS) External capacitor about 0.1uf to 4.7uf
3	CAP+	-	
4	VDD	-	Power supply
5	VSS	-	GND
6	SDA	-	Serial data input
7	SCL	-	Serial clock input
8	RST	-	External reset pin

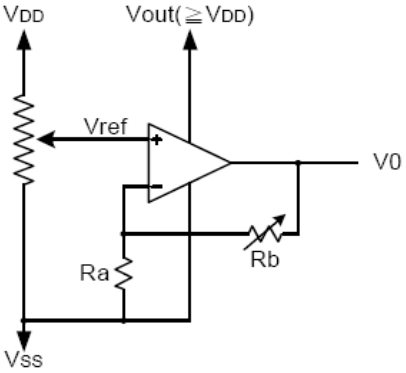
7. Power Supply for LCD Module





2 x step-up voltage relationships

V0 voltage follower value calculation



$$V0=(1+\frac{Rb}{Ra})\times Vref$$

$$While\ Vref=VDD\times(\frac{\alpha+36}{100})$$

C5	C4	C3	C2	C1	C0	α
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

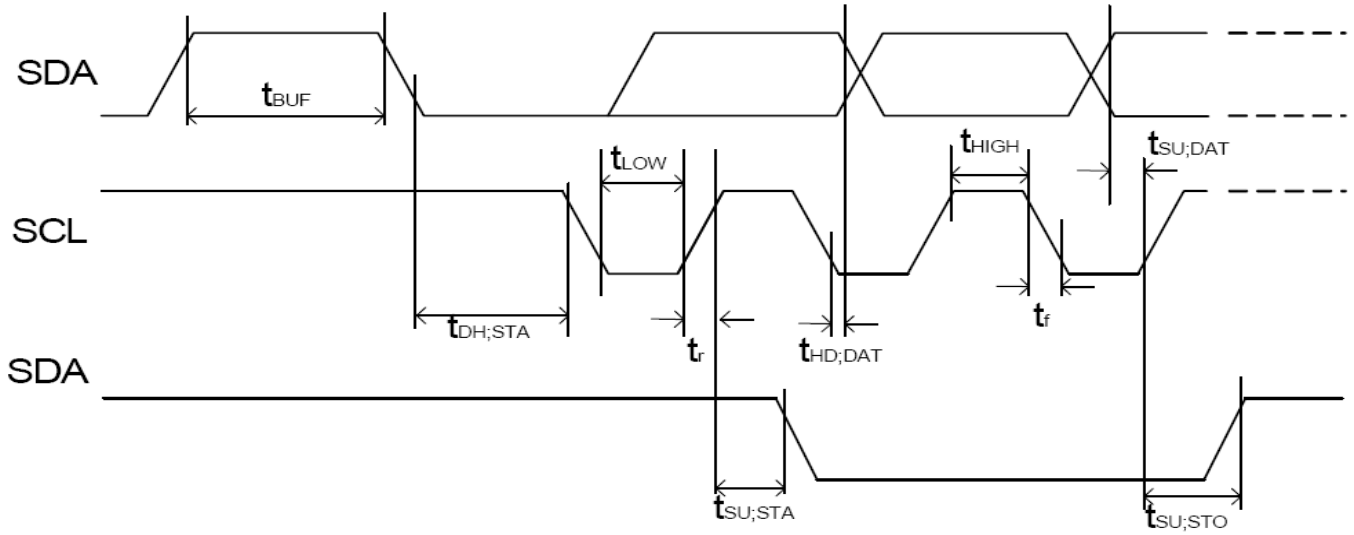
Rab2	Rab1	Rab0	1+Rb/Ra
0	0	0	1
0	0	1	1.25
0	1	0	1.5
0	1	1	1.8
1	0	0	2
1	0	1	2.5
1	1	0	3
1	1	1	3.75

8. Backlight Information

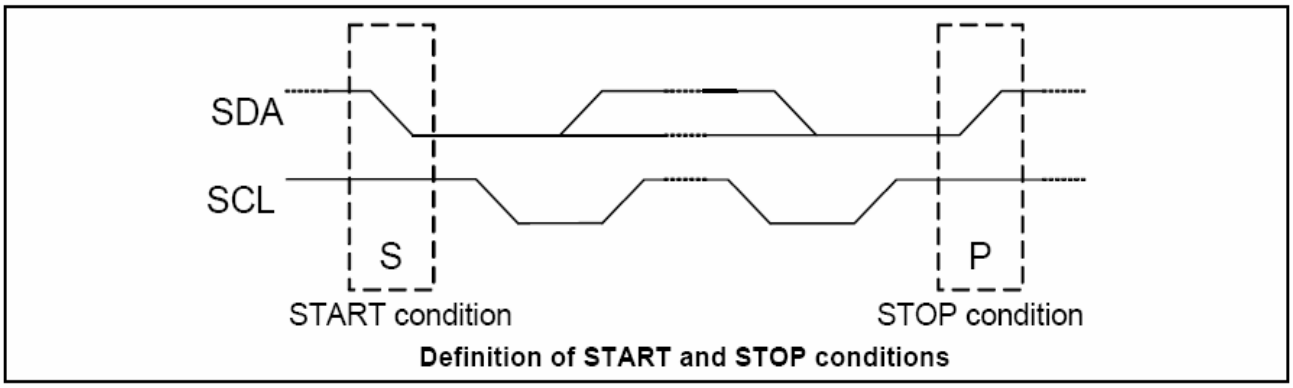
No backlight

9. Timing Characteristics

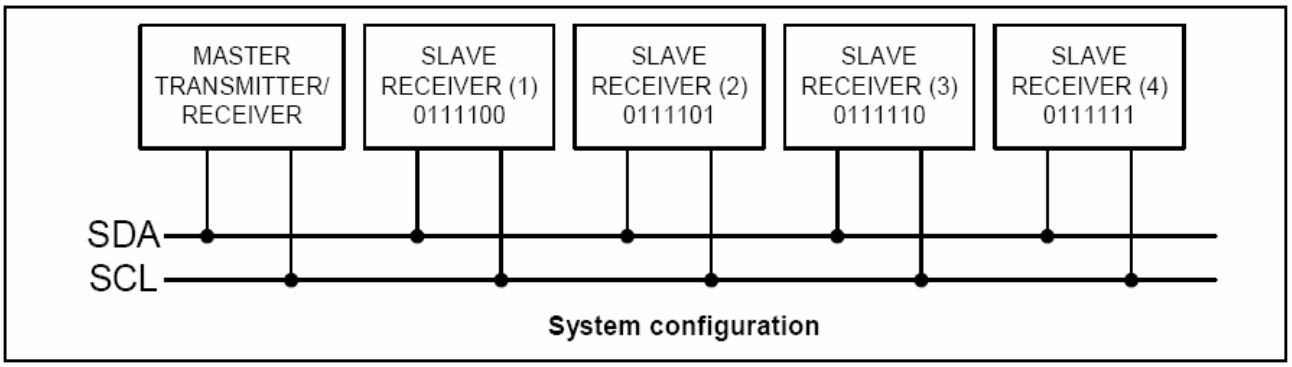
9.1. I2C interface



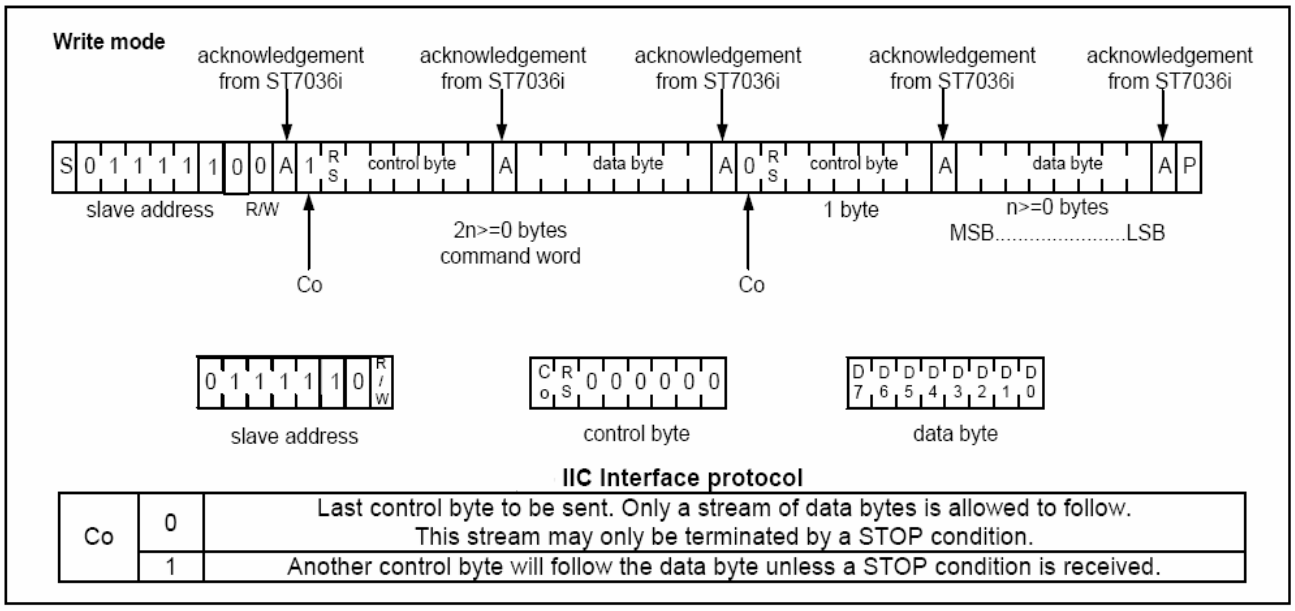
Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	300K	DC	400	kHz
SCL clock low period		t_{LOW}		2.5	—	1.3	—	μs
SCL clock high period		t_{HIGH}		0.6	—	0.6	—	
Data set-up time	SDA	$t_{SU;DAT}$	—	1800	—	700	—	ns
Data hold time		$t_{HD:DAT}$		0	—	0	0.5	μs
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	—	400	—	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	—	0.6	—	μs
Start condition hold time		$t_{HD;STA}$	—	1.8	—	1.0	—	μs
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	—	0.6	—	μs
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	—	1.3	—	μs



Definition of START and STOP conditions



System configuration



IIC Interface protocol

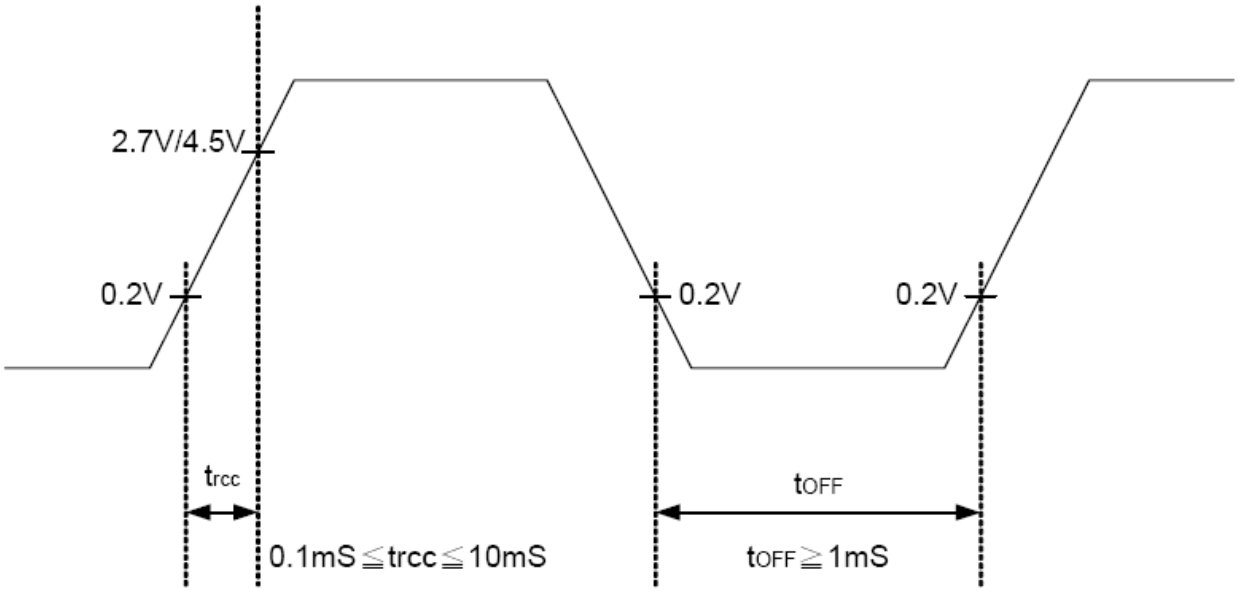
Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

Various kinds of operations according to RS and R/W bits.

9.2. Reset Timing

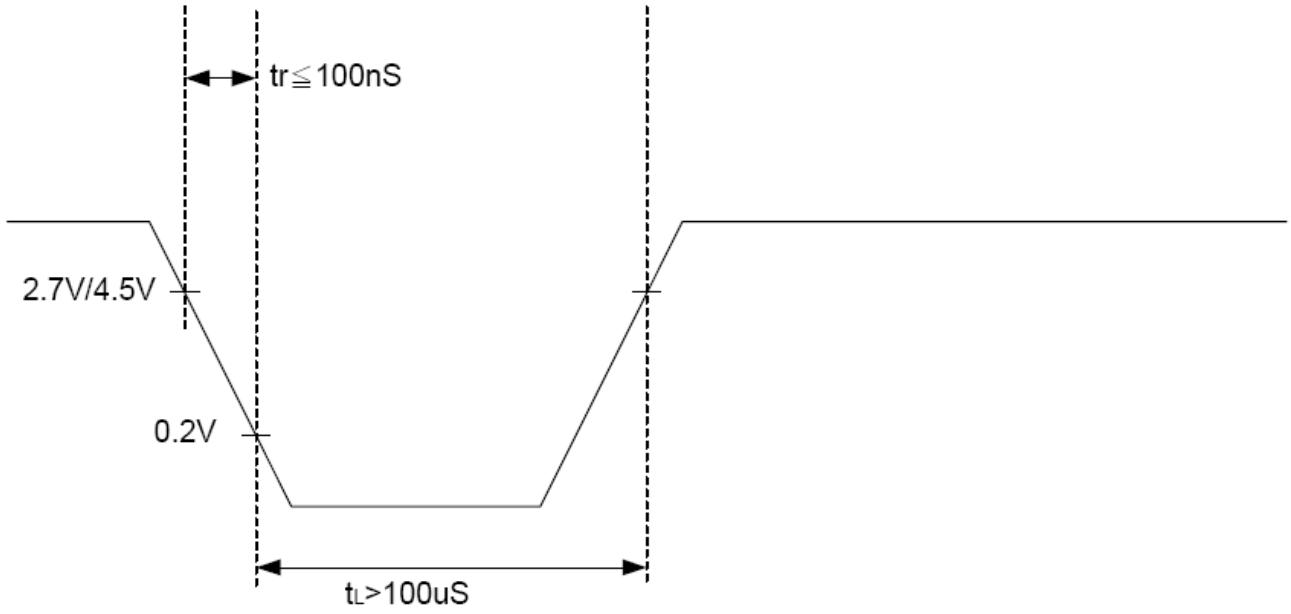
Internal Power Supply Reset



Notes:

- tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation, and at 2.7V for 3V operation.
- For if 2.7V/4.5V is not reached during 3V/5V operation, internal reset circuit will not operate normally.

Hardware reset(XRESET)



10. Instruction Description

➢ **instruction table at "Normal mode"**

(when "EXT" option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 µs	18.5 µs	14.3 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 µs	18.5 µs	14.3 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 µs	18.5 µs	14.3 µs
Function Set	0	0	0	0	1	DL	N	X	X	X	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 µs	18.5 µs	14.3 µs
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs

➢ instruction table at "Extension mode"

(when "EXT" option pin connect to Vss, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 µs	18.5 µs	14.3 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 µs	18.5 µs	14.3 µs
Function Set	0	0	0	0	1	DL	N	DH	IS2	IS1	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS[2:1]: instruction table select	26.3 µs	18.5 µs	14.3 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 µs	18.5 µs	14.3 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 µs	18.5 µs	14.3 µs

Instruction table 0(IS[2:1]=[0,0])														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	**26.3 µs**	**18.5 µs**	**14.3 µs**
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	**26.3 µs**	**18.5 µs**	**14.3 µs**

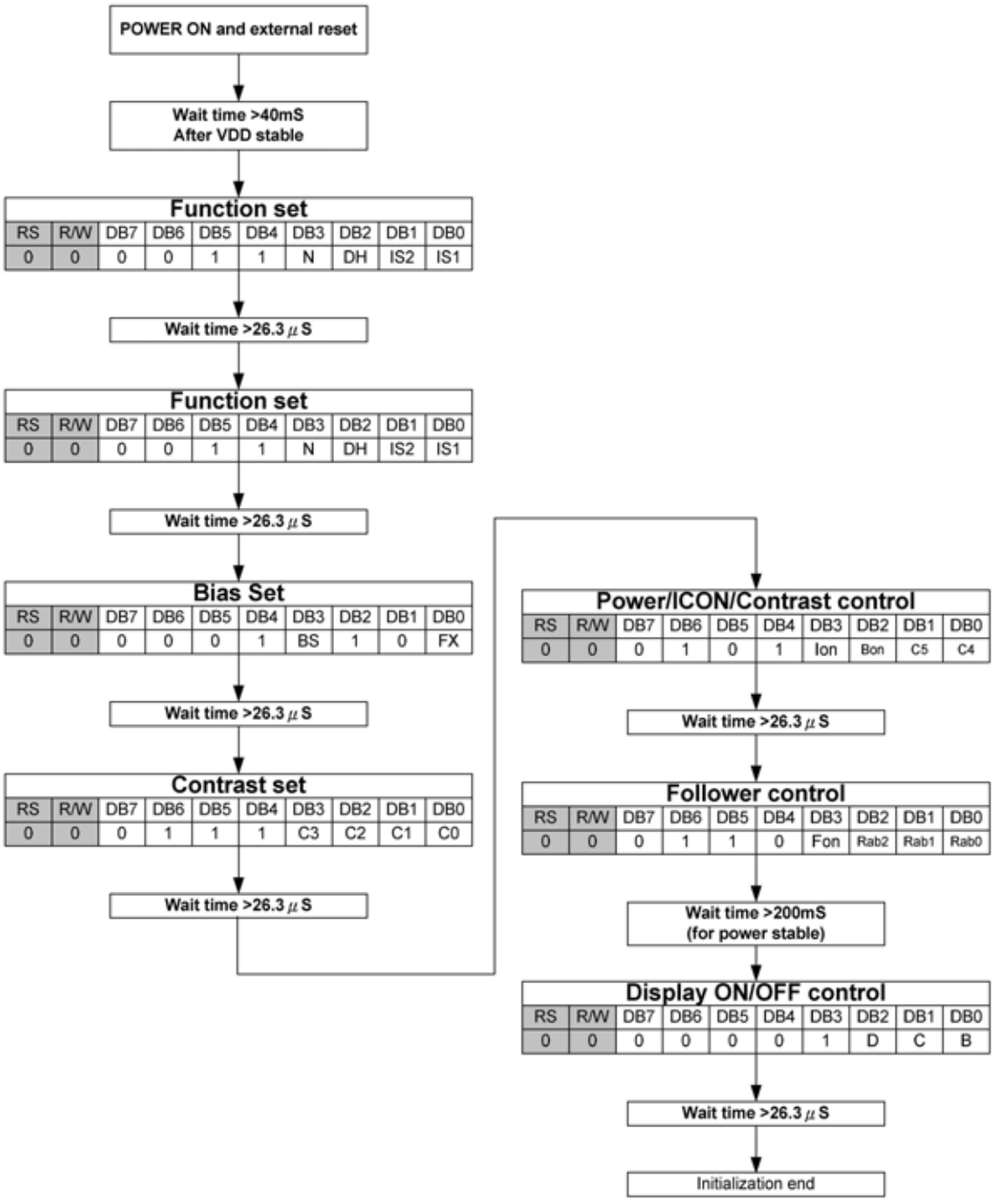
Instruction table 1(IS[2:1]=[0,1])														
Bias Set	0	0	0	0	0	1	BS	1	0	FX	BS=1:1/4 bias BS=0:1/5 bias FX: fixed on high in 3-line application and fixed on low in other applications.	**26.3 µs**	**18.5 µs**	**14.3 µs**
Set ICON Address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	**26.3 µs**	**18.5 µs**	**14.3 µs**
Power/ICON Control/ Contrast Set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	**26.3 µs**	**18.5 µs**	**14.3 µs**
Follower Control	0	0	0	1	1	0	Fon	Rab 2	Rab 1	Rab 0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	**26.3 µs**	**18.5 µs**	**14.3 µs**
Contrast Set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	**26.3 µs**	**18.5 µs**	**14.3 µs**

Instruction table 2(IS[2:1]=[1,0])														
Double Height Position Select	0	0	0	0	0	1	UD	X	x	x	UD: Double height position select	**26.3 µs**	**18.5 µs**	**14.3 µs**
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use (reserved for test)	**26.3 µs**	**18.5 µs**	**14.3 µs**

Instruction table 3(IS[2:1]=[1,1]):Do not use (reserved for test)

11. Initializing by Instruction

- Serial interface & IIC interface (fosc = 380kHz)



12.Font table

13. Quality Assurance

Screen Cosmetic Criteria

No.	Defect	Judgement Criterion	Partition
1	Spots	A)Clear Size:d mm — Acceptable Qty in active area d ≦0.1 — Disregard 0.1<d≦0.2 — 6 0.2<d≦0.3 — 2 0.3<d — 0 Note:Including pin holes and defective dots which must be within one pixel size. B)Unclear Size:d mm — Acceptable Qty in active area d ≦0.2 — Disregard 0.2<d≦0.5 — 6 0.5<d≦0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarizer	Size:d mm — Acceptable Qty in active area d≦0.3 — Disregard 0.3<d≦1.0 — 3 1.0<d≦1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

14. Reliability

■Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 200hrs	-
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10℃ 200hrs	-
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	-
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	-
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	70℃,90%RH 96hrs	-
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40℃,90%RH 96hrs	-
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -10℃ 25℃ 60℃ 30min 5min 30min 1 cycle	-10℃/60℃ 10 cycles	-
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	-
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	-
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	-
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	-

***Supply voltage for logic system=5V. Supply voltage for LCD system = Operating voltage at 25℃

15. Appendix (Drawing)